ISPEC 2025

INDIAN SEMICONDUCTORS & PACKAGING ECOSYSTEM CONFERENCE 2025

4-7 MARCH

Mahatma Mandir, Gandhinagar, Gujarat

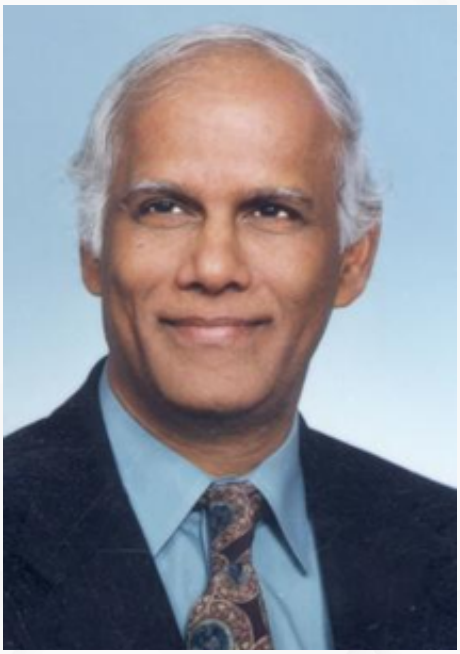
Events

IESA VISION SUMMIT 2025
Date: 5-7 March

GUJARAT SEMICCONNECT
Date: 5-7 March

Co-Organised By

WELCOME TO ISPEC AND WELCOME TO NEW INDIA, A SEMICONDUCTOR NATION



Thanks to the visionary leadership of **Hon'ble Prime Minister Shri Narendra Modi Ji** and **Hon'ble Union Minister of Electronics and Information Technology Shri Ashwini Vaishnaw Ji** and the dedication of distinguished MeitY and ISM Secretaries, Shri S Krishnan, Shri Akash Tripati, and Shri Sushil Pal, India is poised to become a global hub for semiconductors, packaging and systems through their ISM initiative. I'm honored to have been chosen by them as an expert technical advisor and champion to transform Indian electronics in my field of integrated systems; integrating semiconductors, components and packaging.

India has all the fundamentals to be a global leader. It is correcting its two weaknesses in R&D and manufacturing technologies through the ISM initiative. India has a well-educated workforce in basic sciences and engineering, unparalleled expertise, and resources in design and software. Global companies are very much interested in investing in India to design, develop and manufacture high-quality and cost-effective electronic products.

IDSPS (Indian Design, Semiconductors, Packaging and Systems) As a National Initiative

I want to congratulate the ISM team for making the historic semiconductor and package manufacturing happen in India after many trials in the last three decades. The IDSPS program, described here, is being developed to provide a sustainable path for manufacturing and growth of semiconductor industry in India forever.

Summary of the IDSPS Program

- IDSPS is created as a nationwide, 200- person team consisting of 27 IITs and IISc and 80 faculty from these top academic research institutions, and 80 companies from India, the U.S., Europe, Japan, Korea and Taiwan
- IDSPS program is created with four goals to build the nation from ground up for sustainable manufacturing and growth of semiconductor industry in India
    - Leading- edge, next -gen strategic industry-driven research in 12 strategic design, semiconductor, packaging and system technologies
    - Next -gen educated workforce in these 12 strategic technologies
    - Advanced manufacturing materials and tools involving global suppliers
    - Entire supply-chain ecosystem from design to semiconductors to packaging and systems
- We identified four product sectors and 12 strategic research areas to build a sustainable nation with 12 industry-co-development centers (ICC) and industry consortium in each
- About 100 Indian and global companies expressed to co-invest in the 12 centers with industry consortium in each of the 12 SRAs of the IDSPS program
- We estimate to educate about 2000 Ph.D.'s, 3000 MTech and 3000 BTech in next gen technologies as well as educate and train> 10,000 technicians, operators and manufacturing engineers for manufacturing, in addition to re-educating 15,000 industry professionals from other sectors in 10 years **(Fig.1)**

- The 100 industry partners span the entire ecosystem from researchers, developers, suppliers, manufacturers and users from India and the world
- By involvement of global supply-chain companies, the IDSPS program expects to develop advanced materials and tools (advanced manufacturing) to prepare for next gen manufacturing in India
- The 12 SRA faculty and industry technology teams are planning to hold 12 India-wide industry workshops in February-March 2025 to finalize the 12 ICC's with an industry consortium in each and to submit proposals to MeitY and industry partners' funding by March 31, 2025
- The IDSPS team has created the Indian Semiconductors and Packaging Ecosystem Conference (ISPEC) to bring together the entire IDSPS team of researchers, developers, suppliers, manufactures and users. The first ISPEC was held in March 2024 in Chandigarh and the second one is planned in Gandhinagar from March 4-7, 2025

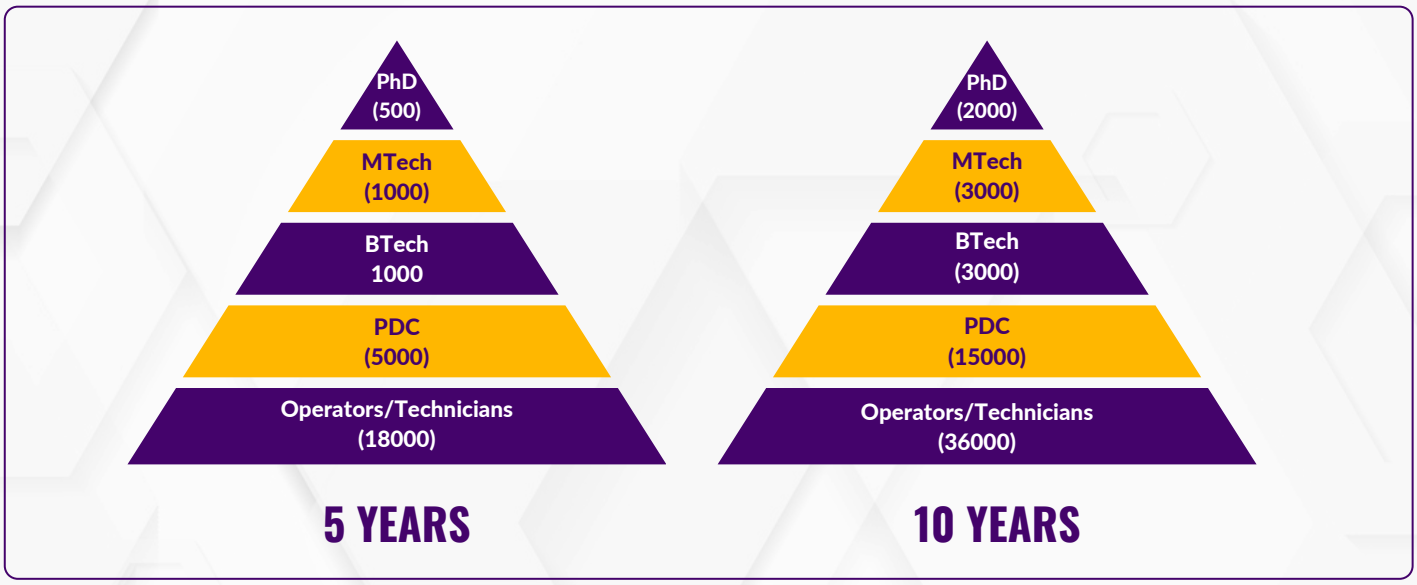


Figure 1: Workforce Development for R&D and Manufacturing (est.)

Technical Vision

A technical vision for India can be semiconductors, packaging or systems, or combining all to form integrated systems, integrating devices and system components into integrated system packages **(Fig. 2)** to serve a variety of strategic needs in four areas:

- Automotive including power electronics with compound semiconductors
- Computing and AI
- 6G and beyond communications, and
- Integrated sensors for IoT, medical and other applications

This integrated systems vision has the best potential to transform India from its current design-centric model at device level to a system-centric model, from system design, fabrication, integration, assembly, and test to form end products that serve both growing domestic and global markets. This is particularly true as the global industry moves into post Moore's Law devices and systems which are currently at < 2nm in R&D and which provide <15% transistor performance improvement from node to node, in contrast to a 35% improvement during the peak of Moore's Law, thus reinforcing the integrated systems vision.

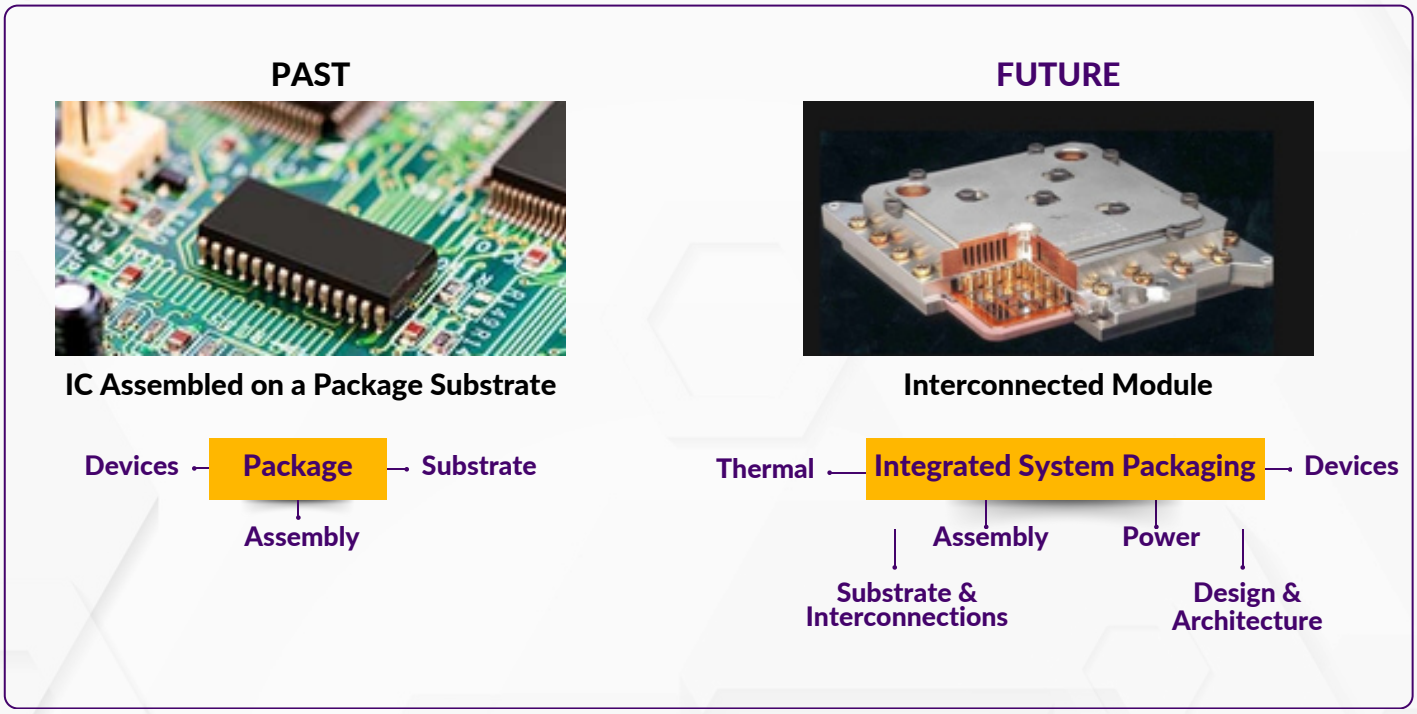


Figure 2: Traditional Packaging vs. Integrated Systems Packaging

IDSPS PROGRAM FOR SUSTAINABLE MANUFACTURING IN INDIA

With the historic success in setting up initial manufacturing plants in India based on 1980 technologies, the IDSPS program, described here, is being developed to bridge the gap between India and advanced countries **(Fig. 3)** to provide a sustainable path for manufacturing and growth of semiconductor industry in India forever by focusing in four areas:

- Design and Technologies (DSPS)
- Educated workforce in technologies and manufacturing
- Advanced Manufacturing: materials, design and process tools
- Global supply-chain ecosystem in India

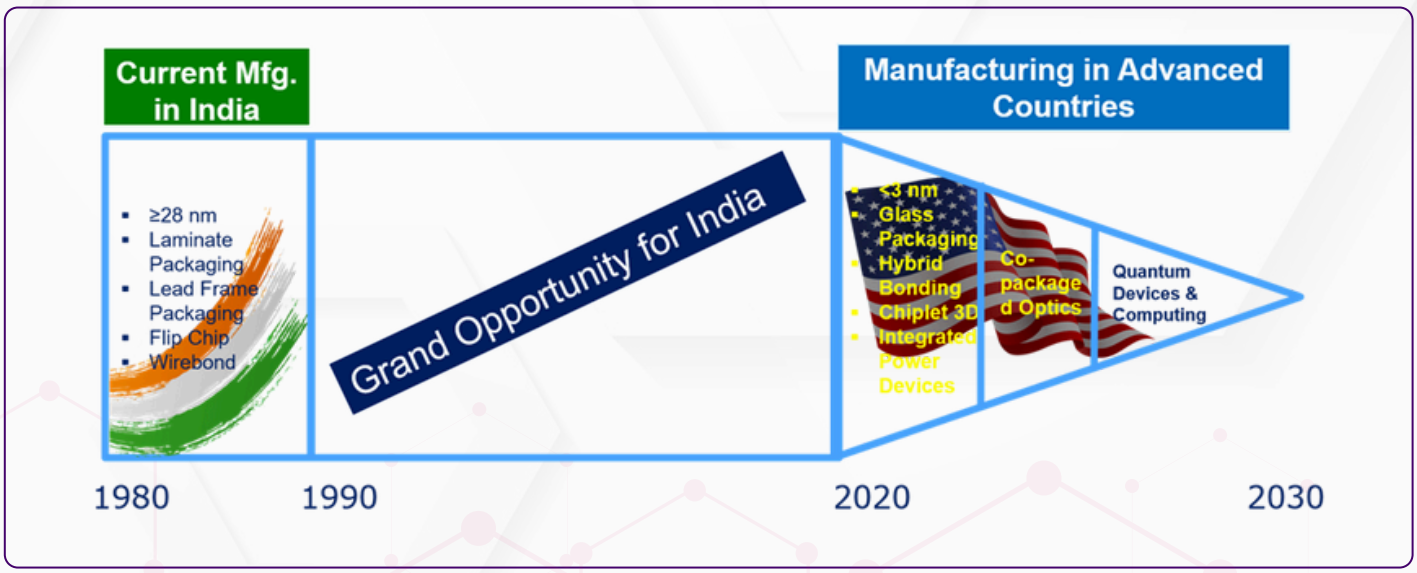


Figure 3: Grand opportunity for Technologies, workforce and supply-chain to bridge the gap between India and advanced countries

Strategy to Attract Global Industry

Most domestic and foreign companies in India today are only focused on design and software. This is a small fraction of India's capabilities. With the new focus on large scale R&D and manufacturing of semiconductors, packaging and systems, India is expected to grow its electronics market by 6-10x in the next ten years. Because of this and other reasons, India expects to be the 3rd largest economy by 2030. In addition, India believes it can be one of the lowest-cost electronics producers. All these are compelling reasons for global industry to invest in R&D, leading to both the development of new technologies and an educated workforce, paving the way for the next generation of manufacturing in India.

All this can happen only if India can attract a large number of global companies to India. The best way for India to attract a large number of global companies is if India **invests in the infrastructure and performs** large scale, global level R&D and workforce developments in all of the strategic system designs and technologies, needed by global companies. This is the first reason. This is beginning to happen with the proposed infrastructure from the government of India. The second reason for global companies to want to come to India is if Indian academic institutions **perform** large scale, global level R&D and workforce development. India is totally capable of these two unlike almost any other country, using its crown jewels—IITs and IISc's, and some private colleges and universities. But this R&D must be at a global level and for the next generation of global industry needs. As well know, the Indian institutions have been producing the very best engineers in the world over the last four decades including those who are now CEOs, CTOs, and technical leaders in many large global companies like IBM, Google, Microsoft, Micron, and Western Digital, to name a few. Their focus of Indian academic institutions so far has been largely on workforce development. In the next phase, they are completely capable of focusing on the two most important ingredients: 1) developing the next generation of technologies the global industry needs and 2) educating students in those technologies that the global industry needs. So, the focus in phase two must be on industry-driven R&D and workforce developments.

Georgia Tech PRC Industry Consortium Model to Transform Indian Semiconductors and Packaging

Traditionally, all top global universities perform high quality academic research addressing scientific and technical challenges that result in educating students, and publications in peer-reviewed journals. A small fraction of these, about 5%, result in discoveries and inventions that end up in products over the next 20 years. So there exist a gap known widely as the **"valley of death"** between academic R&D and industry's need for manufacturing to make competitive products. To address this valley of death gap, many countries have created industrial institutes like Fraunhofer in Germany, ITRI in Taiwan, IME in Singapore and many others to develop industry-needed, ready-to manufacture technologies and transfer these to participating companies. They have been very successful, but their focus is technology development and scale-up, and not research to explore new concepts to make new products. They also don't produce a workforce in any significant way. In the U.S., Semiconductor Research Corporation (SRC) is created to explore new long-term strategic frontiers to provide roadmap solutions for companies. Learning from all these and others, I have created an industry-academic-government (both state and federal) model at Georgia Tech that combines all the above and, in addition, develops programs that produce a large number of well-educated, cross-disciplinary, systems engineers at B.S., M.S. and Ph.D. levels. Georgia Tech was unique in that, it not only explored and demonstrated new individual strategic technologies, but also integrated these technologies into system prototypes and in doing so, educated thousands of engineers at both technology and system integration levels. Georgia Tech is the first and perhaps the only university to have developed this model on such a large scale. But this model required more than faculty and students. It required full-time research faculty and on-campus industry engineers assigned by their global companies and it required state-of-the-art infrastructure to perform leading edge strategic R&D and advanced prototypes in the state-of-the-art experimental and pilot facilities.

As an advisor to ISM, I have begun to apply the Georgia Tech model in India through a 10-step process to set-up an industry consortium for large scale, global level, next generation R&D in 12 strategic research area (SRA) technologies **(Fig. 4)** involving 80 faculty from 27 top IITs, IISc and selective private colleges and universities **(Fig. 5 & 6)**, 24 U.S. academic experts, and 100 global companies. We have made outstanding progress and are ready to set up 12 industry co-development Centers with industry consortium in each in partnership with global companies.

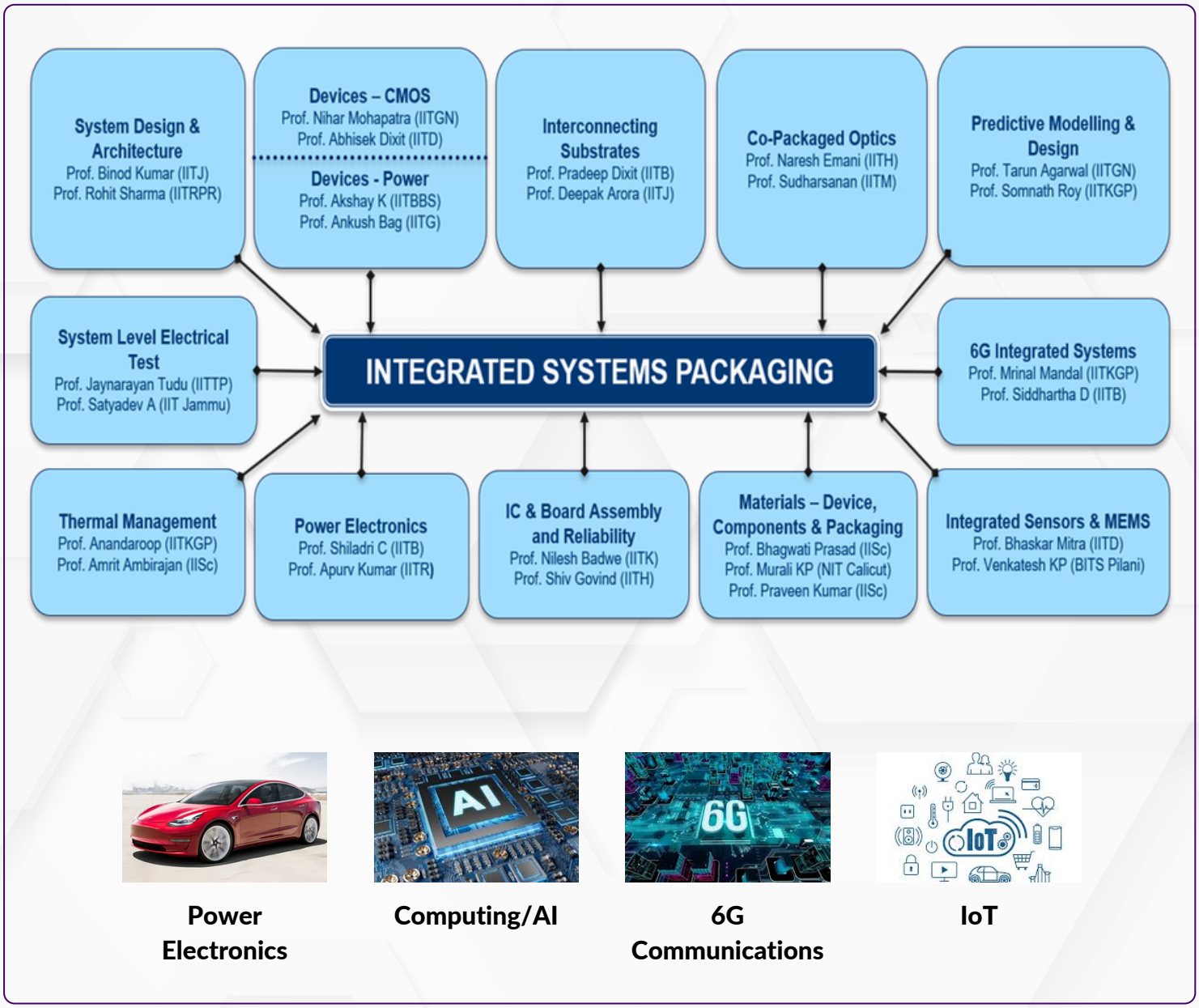


Figure 4: Four Product Sectors and 12 Strategic Research Areas (SRAs)

Research Focus Areas Within Each of The 12 SRAs

Strategic Research Area	Research Focus
Package and System Designs & Architectures Prof. Binod Kumar (IITJ) & Prof. Rohit Sharma (IITRPR)	• High-bandwidth computing • Power efficiency • Privacy, and security • Design for signal, power, EMI, and ESD
Devices: CMOS Prof. Nihar Mohapatra (IITGN) & Prof. Abhisek Dixit (IITD)	• Next-gen (< 3nm) semiconductor materials • Process modeling • Characterization of logic and memory devices
Power Devices Prof. Akshay K (IITBBS) & Prof. Ankush Bag (IITG)	• Device modeling, simulation and design • Substrate and epi growth • Device fabrication and characterization
Package Substrates Prof. Pradeep Dixit (IITB) & Prof. Deepak Arora (IITJ)	• Glass substrates with advances in Package design, embedded components • Large panel lithography • Polymer-Cu RDL to 1 micron
Co-packaged Optics Prof. Naresh E (IITH) & Prof. Sudharsanan S (IITM)	• Design of co-packaged optics for higher bandwidth at lower power than electronic packages • Photonic interconnections • Hybrid bonding assembly • Fiber coupling
Predictive Modeling & Design Prof. Tarun (IITGN) & Prof. Somnath (IITKGP)	• AI assisted design for reliability • Multi-physics design • Materials, interfaces and stress development
6G Integrated Systems Prof. Mrinal Mandal (IITKGP) & Prof. Siddhartha D (IITB)	• Low-loss glass substrates • Embedded devices and components • Package-integrated antennas
Integrated Sensors & MEMS Prof. Bhaskar Mitra (IITD) & Prof. Venkatesh KP (BITS Pilani)	• New concepts in inertial sensors, resonators, printed sensors, 2D materials, sensor fusion.
Materials: Devices, Components & Packaging Prof. Bhagwati P (IISc), Prof. Murali K P (NITC) & Prof. Praveen Kumar (IISc)	• Non-volatile memory • Power components • Package materials
IC & Board Assembly Prof. Nilesh (IITK) & Prof. Shiv Govind (IITH)	• Cu-Cu bonding, sintered Cu die-attach • Fiber coupling assembly
Integrated Power Electronics Prof. Shiladri C (IITB) & Prof. Apurv Kumar (IITR)	• Integrated power modules with advances in system design • Power devices • Integrated packaging • Thermal
Thermal Technologies Prof. Anandaroop B (IITKGP) & Prof. Amrit Ambirajan (IISc)	• Liquid cold plates • 2-phase and boiling heat transfer • Thermal interfaces
System Electrical Test Prof. Jaynarayan T (IITTP) & Prof. Satyadev Ahlawat (IIT Jammu)	• Test advances in chaplet's • 2.5D glass packages • Boundary scan • Analog and mixed signal

New-gen Indian Faculty transforming next-gen R&D and Workforce in Design, Semiconductors, Packaging, and Systems in partnership with 50+ Global Companies

DESIGN & DEVICES

System Design & Architecture
Prof. Binod Kumar (IITJ) &
Prof. Rohit Sharma (IITRPR)

Devices – CMOS
Prof. Nihar Mohapatra (IITGN) &
Prof. Abhisek Dixit (IITD)

Power Devices
Prof. Akshay K (IITBBS) &
Prof. Ankush Bag (IITG)

Integrated Sensors & MEMS
Prof. Bhaskar Mitra (IITD) &
Prof. Venkatesh KP (BITS Pilani)

PACKAGE MATERIALS, SUBSTRATES AND ASSEMBLY

Interconnecting Substrates
Prof. Pradeep Dixit (IITB) &
Prof. Deepak Arora (IITJ)

Co-Packaged Optics
Prof. Naresh E (IITH) &
Prof. Sudharsanan S (IITM)

Predictive Modelling & Design
Prof. Tarun (IITGN) &
Prof. Somnath (IITKGP)

Materials – Devices, Components & Packaging
Prof. Bhagwati P (IISc), Prof. Murali K P (NITC) &
Prof. Praveen Kumar (IISc)

ICBA & Reliability
Prof. Nilesh (IITK) &
Prof. Shiv Govind (IITH)

INTEGRATED PACKAGES, SYSTEMS & TESTS

Power Electronics
Prof. Shiladri C (IITB) &
Prof. Apurv Kumar (IITR)

6G Integrated Systems
Prof. Mrinal Mandal (IITKGP) &
Prof. Siddhartha D (IITB)

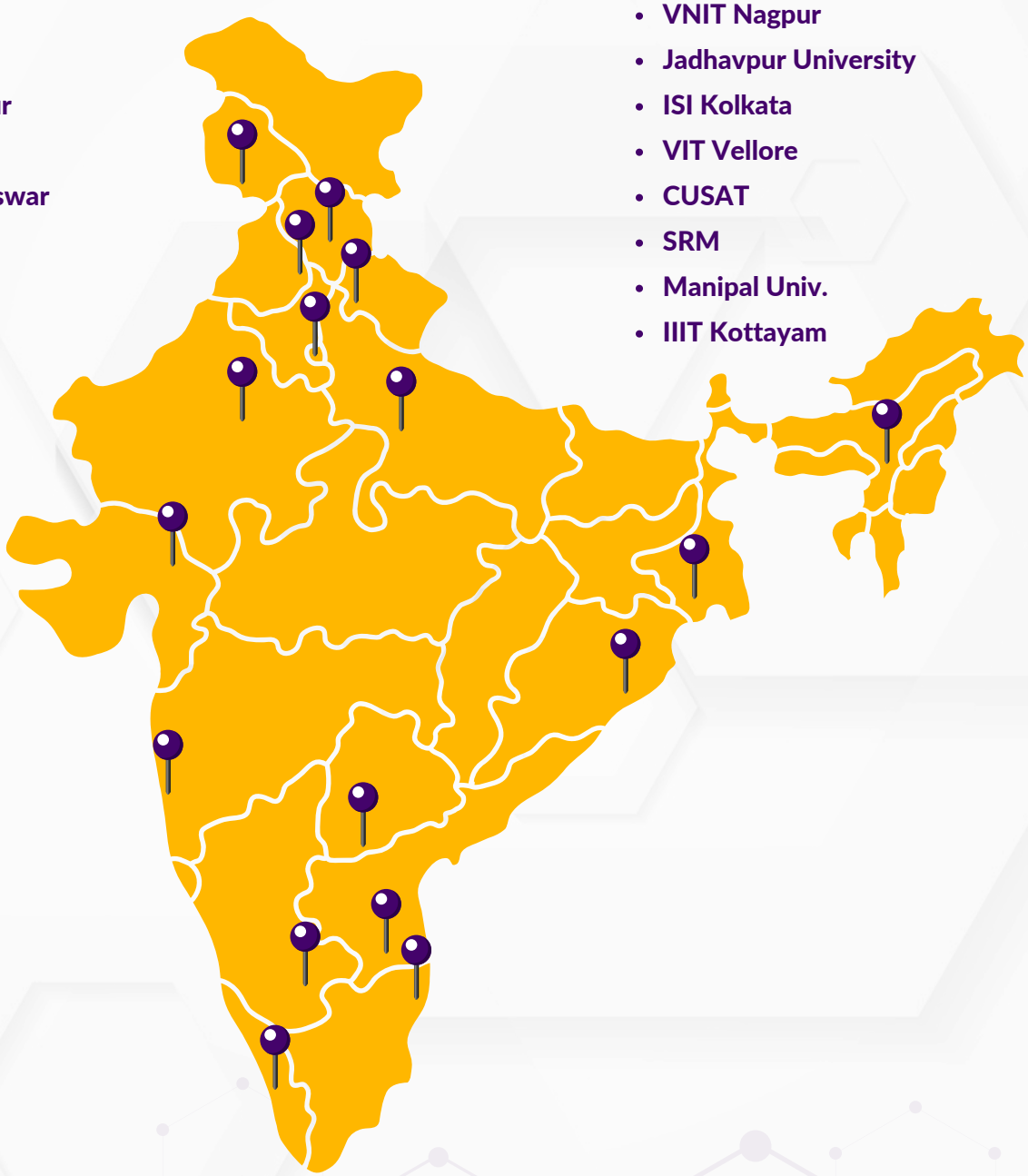
Thermal Management
Prof. Anandaroop B (IITKGP) &
Prof. Amrit Ambirajan (IISc)

System Level Electrical Test
Prof. Jaynarayan T (IITTP) &
Prof. Satyadev Ahlawat (IIT Jammu)

Figure 5: New-gen Indian Faculty transforming next-gen R&D, workforce and supply-chain partnerships

IDSPS FACULTY & INSTITUTIONS

- IISc Bangalore
- IIT Bombay
- IIT Delhi
- IIT Gandhinagar
- IIT Guwahati
- IIT Hyderabad
- IIT Jodhpur
- IIT Kanpur
- IIT Kharagpur
- IIT Madras
- IIT Bhubaneswar
- IIT Tirupati
- IIT Jammu
- IIT Ropar
- IIT Mandi
- IIT Roorkee
- BITS Pilani
- NIT Calicut
- SVNIT
- VNIT Nagpur
- Jadhavpur University
- ISI Kolkata
- VIT Vellore
- CUSAT
- SRM
- Manipal Univ.
- IIIT Kottayam



80+ FACULTY WITH DIVERSE BACKGROUNDS

(ELECTRICAL, MATERIALS, CHEMICAL, MECHANICAL, CHEMISTRY, PHYSICS)

Figure 6: IDSPS Faculty and Institutions for National R&D, Workforce & Supply-Chain

Benefits to Global Industry

There are many benefits to the global industry. The two most important are:

- **Next Gen Workforce:** A large number of well-educated students that are well- prepared in all strategic system design and technologies who can hit the ground running when they join companies upon graduation. A well-educated workforce is the single biggest current barrier to worldwide semiconductor, packaging and systems market growth.
- **Next Generation Industry Needed Technologies:** Large scale R&D, with intellectual property, developed jointly in partnership with the global industry thus addressing the strategic needs of the global industry.

Companies can benefit greatly from these large and historic investments by simply using a small fraction of their CSR funds and by collaborating with Indian faculty and students actively. The best way to begin this journey is by participating in this ISPEC conference. The ISPEC brings and develops a complete ecosystem consisting of researchers, developers, manufacturers, suppliers and users in India. It is also the purpose of the conference for Indian and global collaborating faculty to propose about 150 next generation R&D projects in the 12 SRAs to about 100 participating global companies **(Fig. 7)** that are in attendance.

AMD	VSSC	Wolf Speed	Zestron USA	Murata	Kyocera	Light Speed Photonics Quazar Tech
CSI Talwan	Ansys	Edge Tech	SR	Semicate	NXP	Sicamore Seml
CAT	Denka	VP Seml	Mitsul Chemicals	TDK	$12 Micro Systems	Toyota USA
Linde	Intel	Micron	Sahita Technologies	BHMC	Cisco	Renesas
Qualcomm	Marvell	ROHM	Synopsys	Growel	Higgs Boson Systems L & T SCT	Silitronics
Slemens	Resonac	Stirling	14SI Solutions	Kevin Electrochem	onseml	Rogers
Vedanta	Simm Tech	Yamaha Motor	Baba Fine Chemicals Global Foundries	nanosemic	SIC Power	STARC
Ametek	Westem Digital	Alpha & Omega Semi Evatec	USR Japan	Semicosil	Techsol Engineers	RYZIX
Danfoss	Applied Materials Inc DJK	John Deere	Mbodech	Bosch	Teradyne	Sumibe Japan
Indlum	ISRO	Microsoft	Schott	HCL	Tessolve	Google
LinTec	MELSS	Ruttonsha	Tagore Tech	KNS	Texas Instruments	Kaynes Technology
Reliance Jio	RFIC	Suchi Semicon	Bergensys	Navitas	Tokyo Electron Ltd.	Centum Electronics
Silicon Labs	ST Microelectronics Wipro	Zelas	GMS Indla	Semikron	OMET	Heraeus Electronics
Vishay	Arm	Aark Global Inc	K&S	Cadence	Honeywell	Coming
Analog	AT&S	Ajinomoto	MKS AtoTech	Henkel	Lam Research	BM
Delta Electronics	Dupont	Full Genesem	SCL	Kryvya Semloon	Orbit Solutions	
Infineon	ISRO	JP Data	Tata Electronics	NPL Delhi	SIC Sem	
MacDermid Alpha	Merck	Mitsubishi Electric	Besi	SFO Technologies	Toshiba	

Figure 7: 100 Global Companies Interested in IDSPS Program

ISPEC Conference and Sessions

The ISPEC conference is a five-day program. It begins with 14 professional development courses in all strategic technologies on March 4 at IIT Gandhinagar. The inaugural session on March 5th is a combined session with Vision Summit Conference, followed by many industry, Government and academic keynote talks. Day 2 on March 6 is dedicated to R&D presentations in all 12 SRAs to the global industry by means of 12 presentations and 150 student poster papers from all top research institutions. Day 3 on March 7 starts with three presentations on workforce programs:1) Manufacturing workforce under development, 2) Current DSPS technology workforce programs offered in India and 3) Next gen DSPS workforce programs proposed. The last session brings more than 50 global suppliers from the U.S., Europe, Japan, Korea, Taiwan and Singapore for materials, processes and tools for advanced manufacturing to form next gen integrated systems. The Conference ends with Site Visit to Dholera and Sanand on Mar 7 & 8

Welcome to ISPEC 2025 and welcome to the new semiconductor nation!

Prof. Rao R. Tummala
Champion to build the Nation with R&D, Workforce and Global Supply-chain Partnerships
Emeritus Professor, Georgia Tech
Former IBM Fellow
Advisor to ISM and MeitY, India

OVERVIEW

ISPEC 2025

India's aspiration to become a global hub for semiconductor and package manufacturing requires addressing four critical gaps: research and development (R&D), advanced manufacturing technologies, educated and skilled workforce and global supply chain ecosystem. Supported by a $10 billion incentive package under the India Semiconductor Mission (ISM), the country aims to build a robust ecosystem spanning design, R&D, manufacturing, products, applications, services, and workforce development.

Such a comprehensive ecosystem requires researchers, developers, suppliers of materials and tools, manufacturers, and end-users, all working together. To build the nation in all the above four areas and accelerate progress, the Indian Design, Semiconductor, and Packaging Symposium (IDSPS) initiative has been established. IDSPS is an India-wide program large scale, global level program involving the top 30 top research academic institutions and about 80 global companies, all working together to set up 12 industry-co-development centers with industry consortium in each to close the above four gaps, particularly manufacturing gap In India Vs. advanced countries. The ISPEC brings this entire eco-system community together to review the progress, set up 12ICCs with industry consortium in each.

IESA Vision Summit

Co-located with ISPEC 2.0

A premier industry event, organised annually by the India Electronics & Semiconductor Association(IESA) brings together industry leaders, government officials, innovators, and experts. IESA Vision Summit serves as a platform to explore cutting-edge technologies, emerging trends, and collaborative opportunities that are shaping the future of India's Electronics System Design and Manufacturing (ESDM) sector. This year, the event will be co-located with ISPEC 2.0.

WHAT TO EXPECT

- Keynote talks by Industry, government and academic experts in DSPS technologies
- Plans for 12 industry Co-development centers with industry consortium in each
- Participation by 600+ researchers, developers, suppliers, manufacturers and users
- 150 Student Poster papers from 30 premier research institutions
- 100+ Top global researchers, developers, suppliers, manufacturers, and users from the U.S., Europe, Japan, Korea, Taiwan and India
- 10+ Top Government officials, policy makers
- Corporate executives, technical leaders, Indian and global faculty and students
- 250+ Global Exhibitors to showcase the latest technologies, tools, materials, products, innovations across value chain of Semiconductors, Packaging & Systems.
- 14 Professional Development Courses (PDC) in all next gen technologies by eminent faculty
- 300+ Students and industry professionals taking thePDCs
- Strategic R&D presentations by 80 facultyon all cutting-edge, next gen technologies
- Site Visit to Dholera and Sanand, Gujarat on Mar 7 & 8

POWERING INDIA'S SEMICONDUCTOR REVOLUTION

Next gen research and workforce in Design, Semiconductors, Packaging and Systems:

- Design & Devices
- Materials, Package Substrates & Assembly and test
- Integrated Packages & Systems ; 6G, Power electronics ,Integrated sensors

Research presentations by about 80 faculty in all 12 Strategic Research Areas

Poster Session with 150+ PhD and MTech students and best Poster Awards

Workforce Sessions for:

- Manufacturing Skill Development
- Technology Workforce
- Next-Generation Technology Workforce

Suppliers Session with 50+ global supply chain to kickstart the Indian ecosystem

ISPEC 5-DAY PROGRAM AT A GLANCE

Mar 4	**PDC Courses for Grad Students and Industry Engineers at IIT Gandhinagar**
Mar 5	**Inaugural Session & Keynote Talks at Mahatma Mandir**
Mar 6	**12 Research & 150 Student Poster Papers to set up Industry Centers and Industry Consortium**
Mar 7	**Poster Awards Workforce for Manufacturing, Current & Future Technologies, Global Suppliers & Exhibitors Session**
Mar 8	**Site Visit to Dholera and Sanand, Gujarat**

PDC COURSES FOR GRAD STUDENTS AND INDUSTRY ENGINEERS AT IIT GANDHINAGAR

Design and Devices	
System Design & Architecture	Prof. Binod Kumar (IITJ)
Package Design	Prof. Rohit Sharma (IITRPR)
Devices – CMOS	Prof. Nihar Mohapatra (IITGN)
Devices – Power	Prof. Akshay K (IITBBS)
Integrated Sensors & MEMS	Prof. Bhaskar Mitra (IITD)
Materials, Substrates and Assembly	
Interconnecting Substrates	Prof. Pradeep Dixit (IITB)
Co-Packaged Optics	Prof. Naresh Emani (IITH)
Materials – Device, Components & Packaging	Prof. Bhagwati Prasad (IISc), Prof. Murali KP (NITC) and Prof. Praveen Kumar (IISc)
Predictive Modelling & Design	Prof. Tarun Agarwal (IITGN)
IC & Board Assembly and Reliability	Prof. Nilesh Badwe (IITK)
Integrated Packages, Systems & Tests	
Integrated Power Electronics	Prof. Shiladri Chakraborty (IITB)
Thermal Design & Technologies	Prof. Anandaroop B (IITKGP)
6G Integrated Systems	Prof. Mrinal Mandal (IITKGP)
System Level Electrical Test	Prof. Jaynarayan Tudu (IITTP)

LAST YEAR SPONSORS

ISPEC 2024

Design/EDA

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cadence

Substrates

AT&S

KYOCERA

SIMMTECH

Materials

Ajinomoto

Henkel

Indium Corporation

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mks Atotech

MacDermid Alpha Electronics Solutions

RESONAC Chemistry for Change

TAIYO INK

SUMITOMO BAKELITE CO.,LTD.

IDMs/Fabless

AMD

Analog Devices Ahead of what's possible

IBM

Infineon

intel

NXP

onsemi

Marvell

Qualcomm

Renesas

ST

Texas Instruments

TOYOTA

Western Digital

Equipment

Applied Materials

AAR Global

Besi

CAMECA

AMETEK

DISCO

evatec

HORIBA Semiconductor

Kulicke & Soffa

KEYSIGHT

Lam Research

mks Atotech

Nordson

TOWA

YAMAHA ROBOTICS

ZEISS

Foundry, Assembly & Test

CDIL

CG Power Solutions

GlobalFoundries

HCLTech

KAYNES SEMICON

si2 microsystems

Sahasra

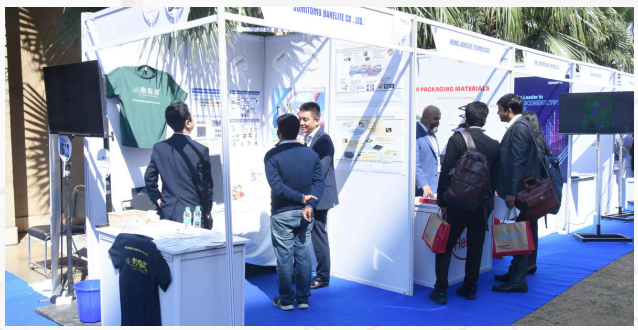
TERADYNE

TATA

TESSOLVE A HERO ELECTRONIX VENTURE

vedanta

LAST YEAR HIGHLIGHTS



BECOME AN EXHIBITOR

Standard Booth* size: 3mX2m

Price: ₹ 50000 Per Sq Meter + Taxes applicable

Includes:

- One table
- Two chairs
- 1KW connection
- Plug point
- Lights (standard fitments)

- Name on Facia and branding on three walls (Printing) is included but design has to be shared by booth owners.
- Rest like TV, Extra Power, Extra furniture etc will be extra

For Booking & Exhibiting Opportunities, contact:

Email Id: davendar.kaul@iesaonline.org
Phone: +91 99110 86154

Email Id: sarva.harish@hyderabad.bits-pilani.org
Phone: +917997865439